AHB5 Protocol

Introduction:

AMBA AHB is a bus interface suitable for high-performance synthesizable designs. It defines the interface between components, such as masters, interconnects, and slaves.

AMBA AHB implements the features required for high-performance, high clock frequency systems including:

- Burst transfers.
- Single clock-edge operation.
- Non-tristate implementation.
- Wide data bus configurations, 64, 128, 256, 512, and 1024 bits.

AHB also supports multi-master designs by the use of an interconnect component that provides arbitration and routing signals from different masters to the appropriate slaves.

Figure 1-1 shows a single master AHB system design with the AHB master and three AHB slaves.

The bus interconnect logic consists of one address decoder and a slave-to-master multiplexor. The decoder monitors the address from the master so that the appropriate slave is selected and the multiplexor routes the corresponding slave output data back to the master.

AHB Block Diagram:

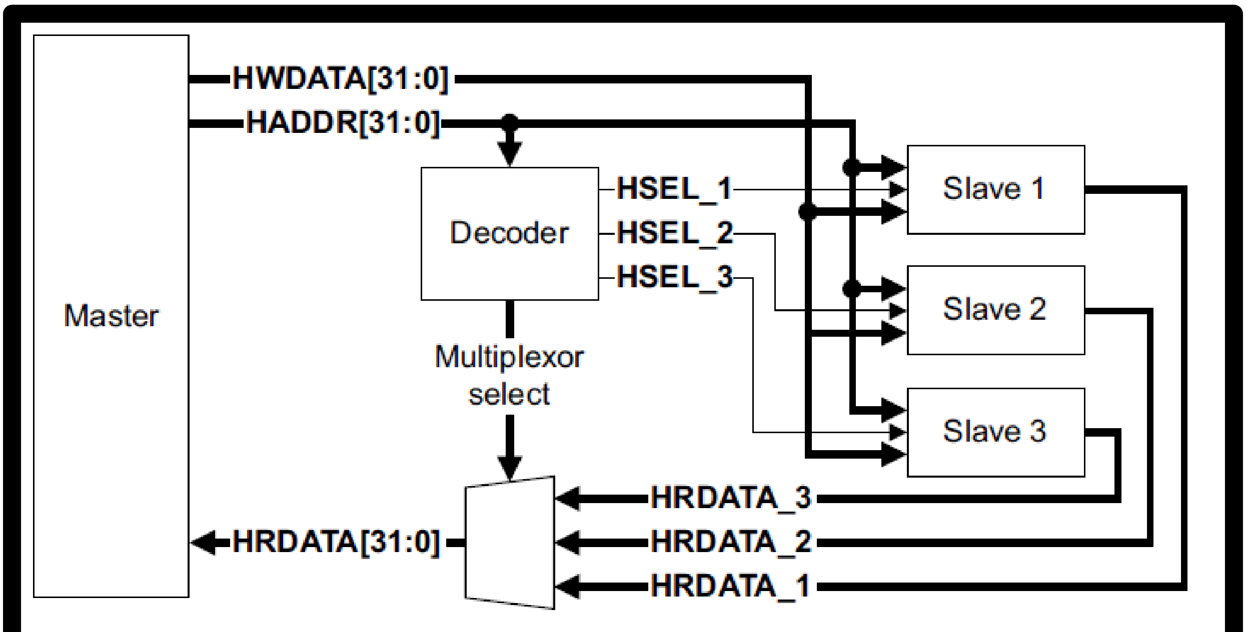

Figure 1-1 AHB block diagram

Master interface:

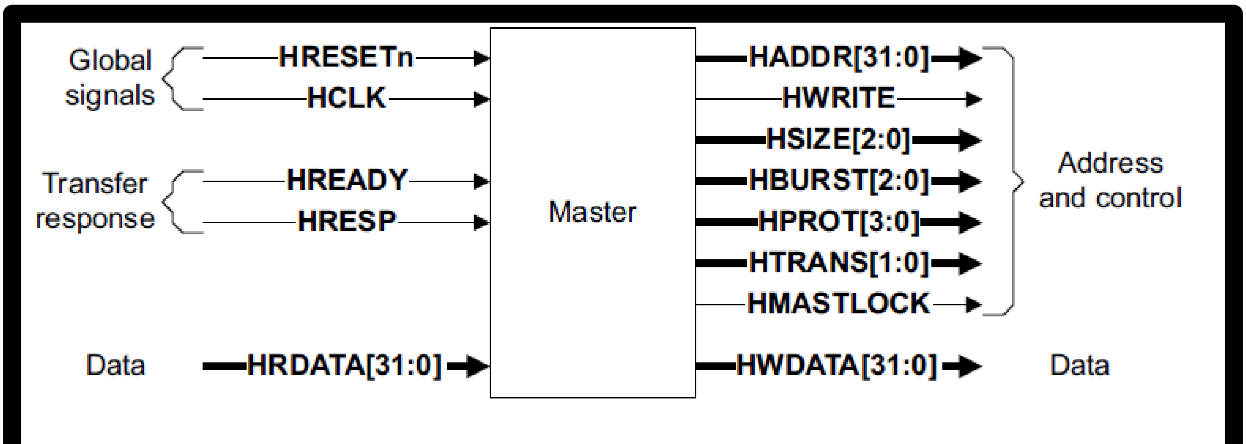

Figure 1-2 Master interface

Slave interface:

- The slave signals back to the master
- The completion or extension of the bus transfer.
- The success or failure of the bus transfer.

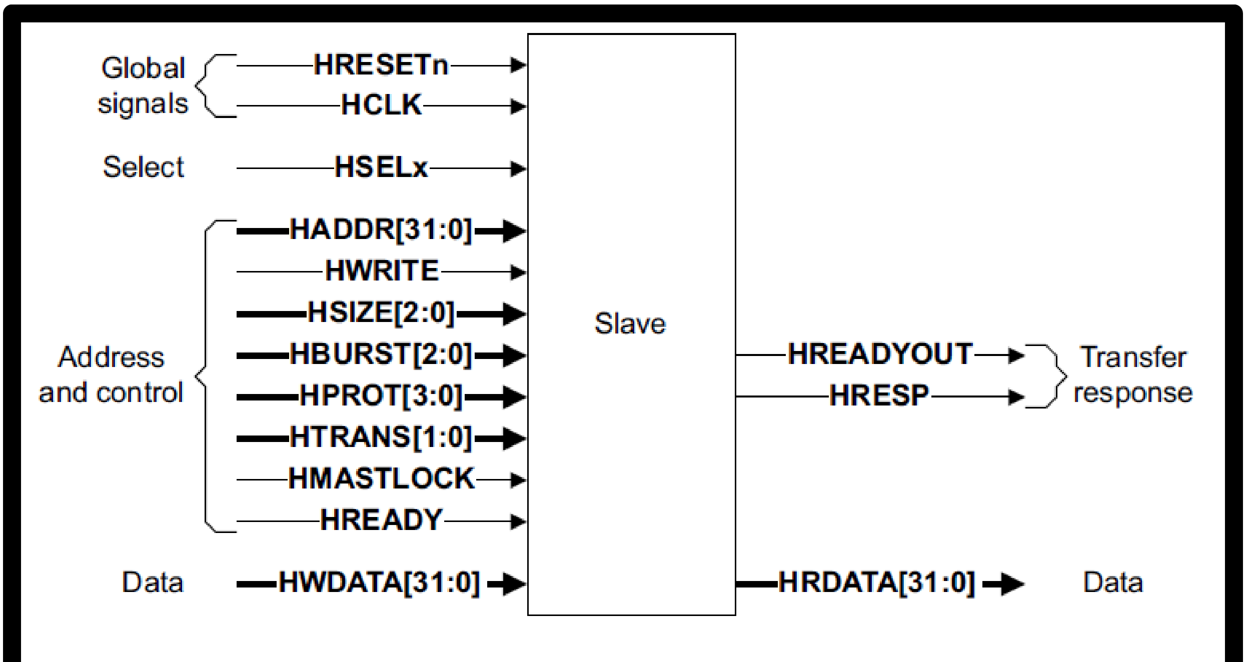

Figure 1-3 Slave interface

Interconnect:

An interconnect component provides the connection between masters and slaves in a system.

A single master system only requires the use of a Decoder and Multiplexor, as described in the following sections.

A multi-master system requires the use of an interconnect that provides arbitration and the routing of signals from different masters to the appropriate slaves. This routing is required for address, control, and write data signaling.

Further details of the different approaches used for multi-master systems, such as single layer or multi-layer interconnects, are not provided within this specification.

Decoder and Multiplexer:

Decoder

This component decodes the address of each transfer and provides a select signal for the slave that is involved in the transfer. It also provides a control signal to the multiplexor.

Multiplexer

A slave-to-master multiplexor is required to multiplex the read data bus and response signals from the slaves to the master. The decoder provides control for the multiplexer.

Operation:

The master starts a transfer by driving the address and control signals. These signals provide information about the address, direction, width of the transfer, and indicate if the transfer forms part of a burst. Transfers can be:

- Single.
- Incrementing bursts that do not wrap at address boundaries.
- Wrapping bursts that wrap at particular address boundaries.

The write data bus moves data from the master to a slave, and the read data bus moves data from a slave to the master.

Every transfer consists of:

- Address phase One address and control cycle.
- Data phase One or more cycles for the data.

HREADY and HRESP:

A slave can request that the master extends the data phase by using HREADY.

This signal, when LOW, causes wait states to be inserted into the transfer and enables the slave to have extra time to provide or sample data. The slave uses HRESP to indicate the success or failure of a transfer.

Signals in AHB5 Protocol:

Name	Source	Description
Global signals		
HCLK	Clock Source	The bus clock times all bus trasfers. All signal timings are related to the rising edge of HCLK
HRESETn	Reset Controller	The bus reset signal is active LOW and resets the system and the bus. This is the only active LOW signal
Master signals		
HADDR[31:0]	Slave and decoder	The 32-bit system address bus
HBURST[2:0]	Slave	The burst type indicates if the transfer is a single transfer r form part of a burst. Fixed length bursts of 4, 8, and 16 beats are supported. The burst can be incrementing or wrapping. Incrementing bursts of undefined length are also supported.
HMASTLOCK	Slave	When HIGH, indicates that the current transfer is part of a locked sequence. It has the same timing as the address and control signals.
HPROT[3:0]	Slave	The protection control signals provide additional information about a bus access and indicate how an access should be handled within a system. The signals indicate if the transfer is an opcode fetch or data access, and if the transfer is a privilleged more access or a user mode access
HPROT[6:4]	Slave	The 3-bit extension of the HPROT signal that adds extended memory types. The signal extension is supported if the AHB5 Extended_Memory_Types property is True
HSIZE[2:0]	Slave	Indicates the size of the transfer, that is typically byte, halfword, or word. The protocol allows for larger sizes up to a maximum of 1024 bits.
HNONSEC	Slave and decoder	Indicates the the current transfer is either a Non-secure or a Secure transfer. The signal is supported if the AHB5 Secure_Transfers property is True.
HEXCL	Exclusive Access Monitor	Exclusive Transfer. Indicates that the transfer is part of an Exclusive access sequence
HMASTER[3:0]	Exclusive Access Monitor and Slave	Master identifier. Generated by a masterif it has multiple Exclusive capable threads. Modified by an interconnect to ensure each master is uniquely identified. This signal is supported if the HAB5 Exclusie_Transfers prperty is True.
HTRANS[1:0]	Slave	Indicates the transfer type of the current transfer. This can be: 1. IDLE 2. BUSY 3. NONSEQUENTIAL 4. SEQUENTIAL
HWDATA[31:0]	Slave	The write data bus transfers data from the master to the slaves during write operations. A minimum daa bus width of 32 bits is recommended. However, this can be extended to enable higher bandwidth operation.
HWRITE	Slave	Indicates the transfer direction. When HIGH this signal indicates a write transfer and when LOW a read transfer. It has the same timing as the address signals, however, it must remain constant throughout a burst transfer
Slave signals		
HRDATA[31:0]	Multiplexer	During read operations, the read data bus transfers data from the selected slave to the multiplexer. The multiplexer then transfers the data to the master. A minimum data bus width of 32 bits is recommended. However, this can be extended to enable higher bandwidth operation.
HREADYOUT	Multiplexer	When HIGH, the HREADYOUT signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer
HRESP	Multiplexer	The transfer response, after passing through the multiplexer, provides the master with additional information on the status of a transfer. When LOW, the HRESP signal indicates that the transfer status is OKAY When HIGH, the HRESP signal indicates that the transfer status is ERROR
HEXOKAY	Multiplexer	Exclusive Okay. Indicates the success of failure of an Exclusive Transfer. The signal is supported if the AHB5 Exclusive_Transfers property is True.
Decoder signals		
HSELx	Slave	Each slave has its own slave select signal HSELx and this signal indicates that the current transfer is intended for the selected slave. When the slave is initially selected, it must also monitor the status of HREADY to ensure that the previous bus transfer has completed, before it responds to the current transfer. The HSELx signal is a combinatorial decode of the address bus
Multiplexer signals		
HRDATA[31:0]	Master	Read data bus, selected by the decoder
HRADY	Master and Slave	When HIGH, the HREADY signal indicates to the master and all slaves, that the previous transfer is complete.
HRESP	Master	Transfer response, selected by the decoder
HEXOKAY	Master	Exclusive okay, selected by the decoder

Basic Transfers:

A transfer consists of two phases:

- Address Lasts for a single HCLK cycle unless its extended by the previous bus transfer.
- Data Might require several HCLK cycles. Use the HREADY signal to control the number of clock cycles required to complete the transfer.

HWRITE controls the direction of data transfer to or from the master. Therefore, when:

- HWRITE is HIGH, it indicates a write transfer and the master broadcasts data on the write data bus, HWDATA[31:0]
- HWRITE is LOW, a read transfer is performed and the slave must generate the data on the read data bus, HRDATA[31:0].

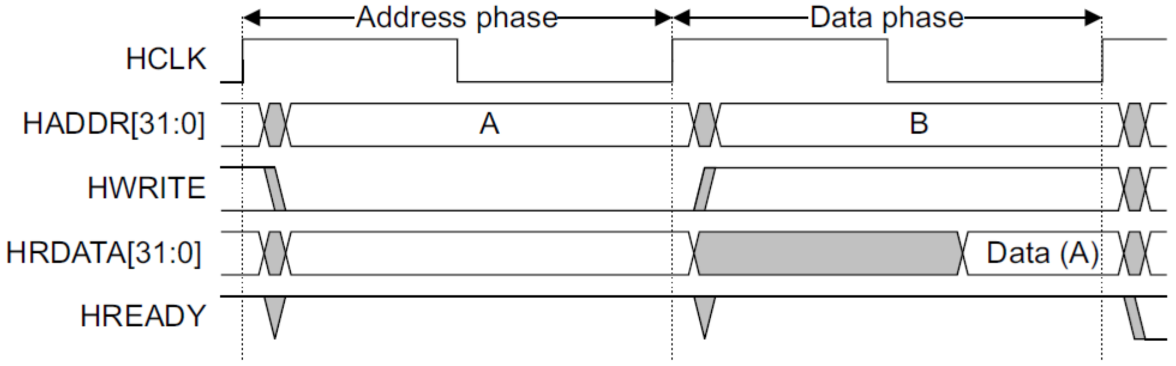

Figure 3-1 Read transfer

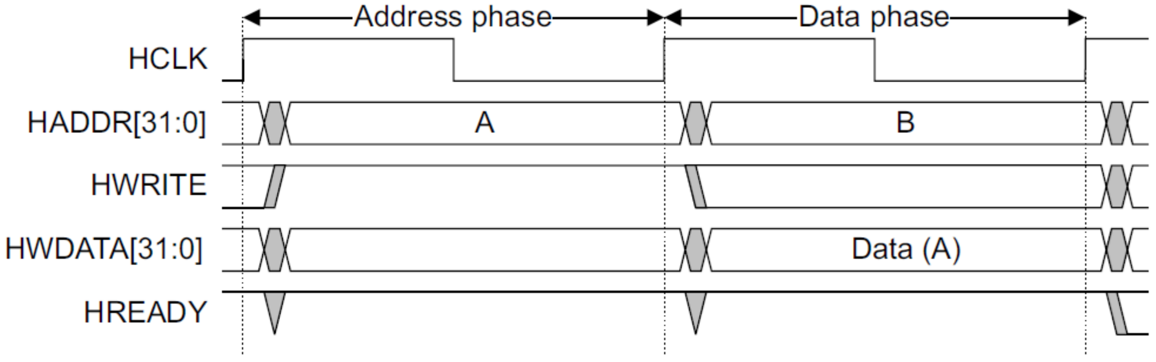

Figure 3-2 Write transfer

Transfer Types:

Table 3-1 Transfer type encoding

HTRANS[1:0]	Type	Description
0b00	IDLE	Indicates that no data transfer is required. A master uses an IDLE transfer when it does not want to perform a data transfer. It is recommended that the master terminates a locked transfer with an IDLE transfer. Slaves must always provide a zero wait state OKAY response to IDLE transfers and the transfer must be ignored by the slave.
0b01	BUSY	The BUSY transfer type enables masters to insert idle cycles in the middle of a burst. This transfer type indicates that the master is continuing with a burst but the next transfer cannot take place immediately. When a master uses the BUSY transfer type the address and control signals must reflect the next transfer in the burst. Only undefined length bursts can have a BUSY transfer as the last cycle of a burst. See *Burst termination after a BUSY transfer* on page 3-35. Slaves must always provide a zero wait state OKAY response to BUSY transfers and the transfer must be ignored by the slave.
0b10	NONSEQ	Indicates a single transfer or the first transfer of a burst. The address and control signals are unrelated to the previous transfer. Single transfers on the bus are treated as bursts of length one and therefore the transfer type is NONSEQUENTIAL.
0b11	SEQ	The remaining transfers in a burst are SEQUENTIAL and the address is related to the previous transfer. The control information is identical to the previous transfer. The address is equal to the address of the previous transfer plus the transfer size, in bytes, with the transfer size being signaled by the **HSIZE[2:0]** signals. In the case of a wrapping burst the address of the transfer wraps at the address boundary.

Transfer Size:

Table 3-2 Transfer size encoding

HSIZE[2]	HSIZE[1]	HSIZE[0]	Size (bits)	Description
0	0	0	8	Byte
0	0	1	16	Halfword
0	1	0	32	Word
0	1	1	64	Doubleword
1	0	0	128	4-word line
1	0	1	256	8-word line
1	1	0	512	-
1	1	1	1024	-

Burst Operation:

Table 3-3 Burst signal encoding

HBURST[2:0]	Type	Description
0b000	SINGLE	Single transfer burst
0b001	INCR	Incrementing burst of undefined length
0b010	WRAP4	4-beat wrapping burst
0b011	INCR4	4-beat incrementing burst
0b100	WRAP8	8-beat wrapping burst
0b101	INCR8	8-beat incrementing burst
0b110	WRAP16	16-beat wrapping burst
0b111	INCR16	16-beat incrementing burst

Protection Control:

Table 3-4 Protection signal encoding

HPROT[3] Modifiable	HPROT[2] Bufferable	HPROT[1] Privileged	HPROT[0] Data/Opcode	Description
-	-	-	0	Opcode fetch
-	-	-	1	Data access
-	-	0	-	User access
-	-	1	-	Privileged access
-	0	-	-	Non-bufferable
-	1	-	-	Bufferable
0	-	-	-	Non-cacheable
1	-	-	-	Cacheable

Memory Types:

Table 3-5 Meaning of the HPROT bits

Bit	Name	Description
HPROT[0]	Data/Inst	When asserted, this bit indicates the transfer is a data access. When deasserted this bit indicates the transfer is an instruction fetch.
HPROT[1]	Privileged	When asserted, this bit indicates the transfer is a privileged access. When deasserted this bit indicates the transfer is an unprivileged access.
HPROT[2]	Bufferable	If both of **HPROT[4:3]** are deasserted then, when this bit is: • Deasserted, the write response must be given from the final destination. • Asserted, the write response can be given from an intermediate point, but the write transfer is required to be made visible at the final destination in a timely manner.
HPROT[3]	Modifiable	When asserted, the characteristics of the transfer can be modified. When deasserted the characteristics of the transfer must not be modified.
HPROT[4]	Lookup	When asserted, the transfer must be looked up in a cache. When deasserted, the transfer does not need to be looked up in a cache and the transfer must propagate to the final destination.
HPROT[5]	Allocate	When asserted, for performance reasons, this specification recommends that this transfer is allocated in the cache. When deasserted, for performance reasons, this specification recommends that this transfer is not allocated in the cache.
HPROT[6]	Shareable	When asserted, indicates that this transfer is to a region of memory that is shared with other masters in the system. A response for the transfer must not be provided until the transfer is visible to other masters. When deasserted, indicates that this transfer is Non-shareable and the region of memory is not shared with other masters in the system. A response for the transfer does not guarantee the transfer is visible to other masters.

Slave Transfer Responses:

Table 5-2 Combined HRESP and HREADYOUT signal response

	HREADYOUT	
HRESP	0	1
0	Transfer pending	Successful transfer completed
1	ERROR response, first cycle	ERROR response, second cycle

Narrow slave on a wide bus:

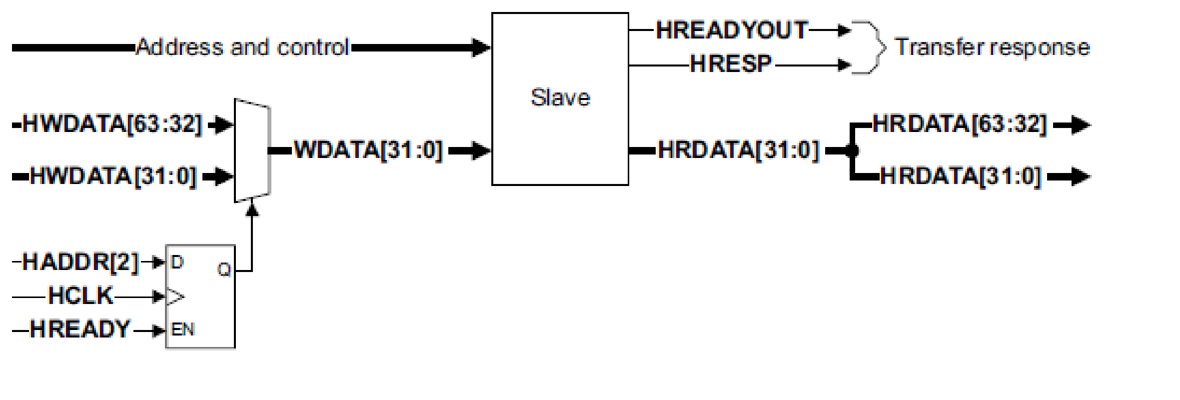

Figure 6-2 Narrow slave on a wide bus

Wide slave on a narrow bus:

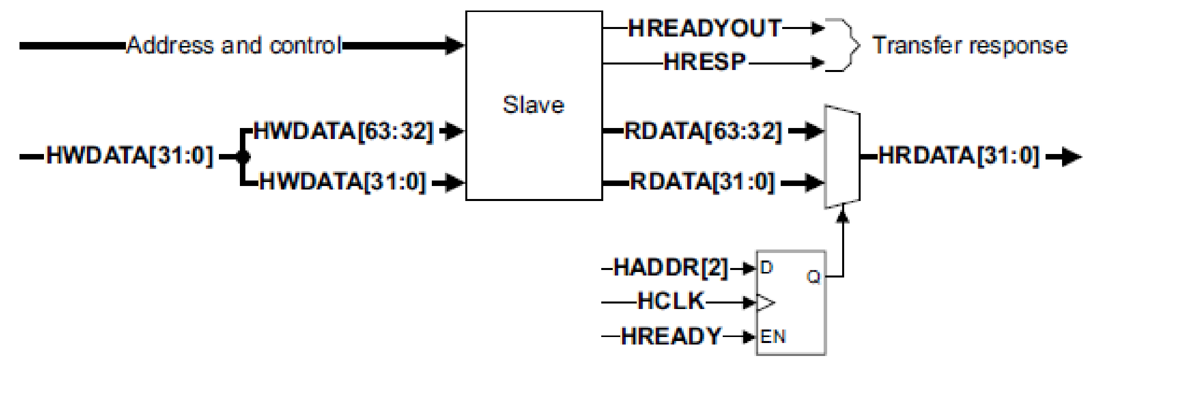

Figure 6-3 Wide slave on a narrow bus

Reset Signal:

The reset signal, HRESETn, is the only active LOW signal in the protocol and is the primary reset for all bus elements. The reset can be asserted asynchronously, but is deasserted synchronously after the rising edge of HCLK.

During reset all masters must ensure the address and control signals are at valid levels and that HTRANS[1:0] indicates IDLE.

During reset all slaves must ensure that HREADYOUT is HIGH.